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714	718
Class	Subclass
ISSUE CLASSIFICATION	

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PATENT NUMBER

U.S. REISSUE Patent Application

O.I.P.E. <i>FA SCANNED AG. 3. 95</i>	O.G. PUBLICATION DATE <i>8-14-01</i>	REISSUE PATENT DATE
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APPLICATION NO. 09/871978	CONT/PRIOR D	CLASS 714	SUBCLASS 718	ART UNIT 2133	EXAMINER Ton 73427
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APPLICANTS

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· Semiconductor integrated circuit comprising synchronous DRAM core and logic circuit integrated into a single chip and method of testing the synchronous DRAM core

PTO-2040
12/99

SURRENDER OF ORIGINAL PATENT _____ (Ex. Initials) ORIGINAL PATENT NUMBER _____

ISSUING CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)					
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
714	718						
INTERNATIONAL CLASSIFICATION		G 06 F 11/00					
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<input type="checkbox"/> TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims 18	Print Claim for O.G. 1
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	(Assistant Examiner) _____ (Date) _____			NOTICE OF ALLOWANCE MAILED	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent No. _____				ISSUE FEE	
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.	(Primary Examiner) _____ (Date) _____			Amount Due	Date Paid
FINAL SPRE REVIEW				ISSUE BATCH NUMBER	
(INITIALS) _____ (Legal Instruments Examiner) _____ (Date) _____					

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